LISTING OF CLAIMS:

1. (Previously presented) A transmitter for use in a communication system, the transmitter comprising a digital input, a coding device for generating data bits for transmission, and means for transmitting the data bits during respective frames of a transmission channel, wherein the coding device comprises a coding circuit for generating a coded output having a greater number of bits than the digital input, an interleaving circuit for operating on the coded output to generate a data block comprising a plurality of interleaved words, a rate matching circuit for adjusting the number of bits in the data block using a rate matching pattern to provide data bits, and means for selecting the rate matching pattern depending on an associated bit deletion or repetition pattern that is selected to ensure that the deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

2. (Canceled)

3. (Previously presented) A transmitter as claimed in claim 1, wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the rate matching pattern of an adjacent interleaved word or words within the block.

4. (Previously presented) A transmitter as claimed in claim 1, wherein the rate matching pattern is selected as a function of an interleaving depth of the interleaving circuit.

Claims 5-10. (Canceled)

11. (Previously presented) A transmitter as claimed in claim 1, wherein the coding circuit applies convolutional coding and said means for selecting selects said rate matching pattern as a function of a constraint length of the convolutional code.

12. (Previously presented) A transmitter as claimed in claim 1, further comprising additional coding devices, each for coding a respective digital input, and a multiplexer for combining output data words of said coding device and said additional coding devices for subsequent transmission by the means for transmitting on a single transmission channel.

13. (Previously presented) A transmitter as claimed in claim 12, wherein outputs of said coding device and said additional coding devices are selected to have different data rates, the combined data rate corresponding to a channel capacity of the transmission channel.

14. (Previously presented) A transmitter as claimed in claim 1, wherein the rate matching pattern forms a matrix including change bits that indicate a change of corresponding bits of said interleaved words within said data block, wherein each row of said matrix includes a maximum of one of said change bits.

15. (Previously presented) A transmitter as claimed in claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source.

16. (Previously presented) A transmitter as claimed in claim 1, wherein said interleaving circuit is not adaptive.

17. (Previously presented) A transmitter as claimed in claim 1, wherein said interleaving circuit has a constant input bit rate.

18. (Previously presented) A transmitter as claimed in claim 1, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source, and wherein said interleaving circuit is not adaptive.

19. (Previously presented) A transmitter as claimed in claim 1, wherein said rate matching circuit alters a coding rate of said coding circuit according to the bit deletion or repetition pattern.

20. (Previously presented) A receiver for use in a communication system, the receiver comprising means for receiving a coded digital signal comprising a received data block comprising a plurality of interleaved words, the data block having been obtained from a digital input, and processed by a coding device to adjust the number of bits in the data block according to a rate matching pattern, the receiver further comprising a data reconstruction circuit having means for adjusting the number of bits in the data block to reverse the action of the coding device, thereby reconstructing the interleaved words, a de-interleaving circuit having means for generating each of the plurality of interleaved words, a channel decoder, and means for selecting the rate matching pattern as a function of an associated bit deletion or repetition pattern having been selected to

ensure that deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

21. (Previously presented) A receiver as claimed in claim 20, wherein the rate matching pattern forms a matrix including change bits that indicate a change of corresponding bits of said interleaved words within said received data block, wherein each row of said matrix includes a maximum of one of said change bits.

22. (Previously presented) A receiver as claimed in claim 20, wherein said coding device has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source.

23. (Previously presented) A receiver as claimed in claim 20, wherein said de-interleaving circuit is not adaptive.

24. (Previously presented) A receiver as claimed in claim 20, wherein said de-interleaving circuit has a constant bit rate.

25. (Previously presented) A receiver as claimed in claim 20, wherein said coding device has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source, and wherein said de-interleaving circuit is not adaptive.

26. (Previously presented) A receiver as claimed in claim 20, wherein a coding rate of said coding circuit is altered according to the bit deletion or repetition rate.

27. (Previously presented) A method of operating a transmitter for use in a communication system, the method comprising operating on a digital input to generate a coded output having a greater number of bits than the digital input, operating on the coded output to generate a data block comprising a plurality of interleaved words and adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, wherein the rate matching pattern is selected as a function of an associated bit deletion or repetition pattern that is selected to ensure that the deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

28. (Previously presented) A method of operating a receiver for use in a communication system, the method comprising receiving a coded digital signal comprising a received data block comprising a plurality of interleaved words, the data block having been obtained from a digital input, and processed to adjust the number of bits in the data block, adjusting the number of bits in the data block according to a rate matching pattern, thereby reconstructing the interleaved words, and de-interleaving and decoding the words to generate an output digital signal, wherein the rate matching pattern is selected as a function of an associated bit deletion or repetition pattern having been selected to ensure that the deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed.

29. (Previously presented) A transmitter as claimed in claim 1, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

30. (Previously presented) A receiver as claimed in claim 20, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

31. (Previously presented) The method of claim 27, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

32. (Previously presented) The method of claim 28, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.